3D Electronics andTrack triggers for CMS

Bejing/Fermilab/Argonne/Chicago Meeting
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3D Electronics Technology

VIP 3D Chip

Oxide Bonding

CMS Tracking Trigger

Large Area Arrays

Conclusions and Prospects

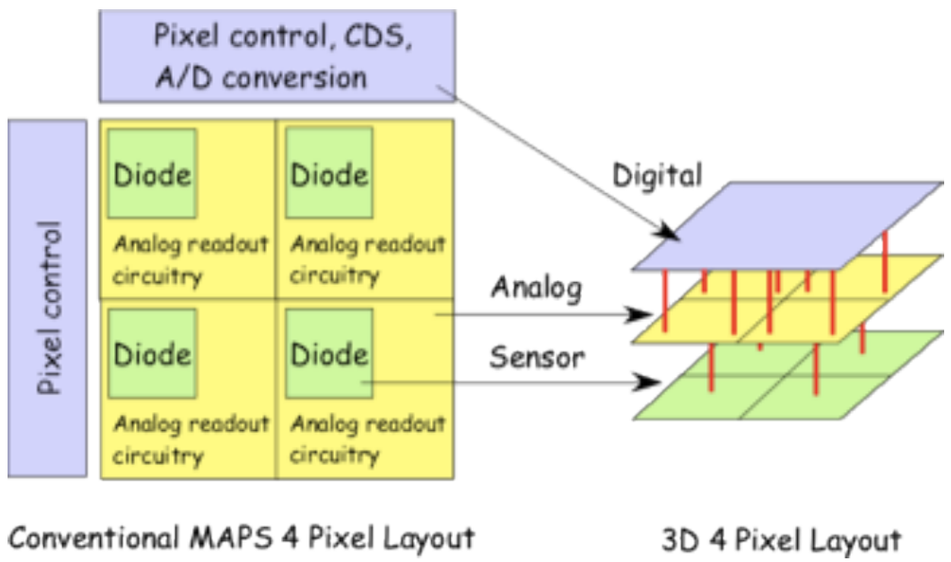
3D Circuits

3D circuits are a major thrust for the IC industry

- They allow bonding of multiple layers of ICs in an single stack - increasing speed, reducing inductance and capacitance
- New technologies for wafer bonding, thinning, interconnect

They have transformative applications in HEP, and will change the way we design silicon tracking

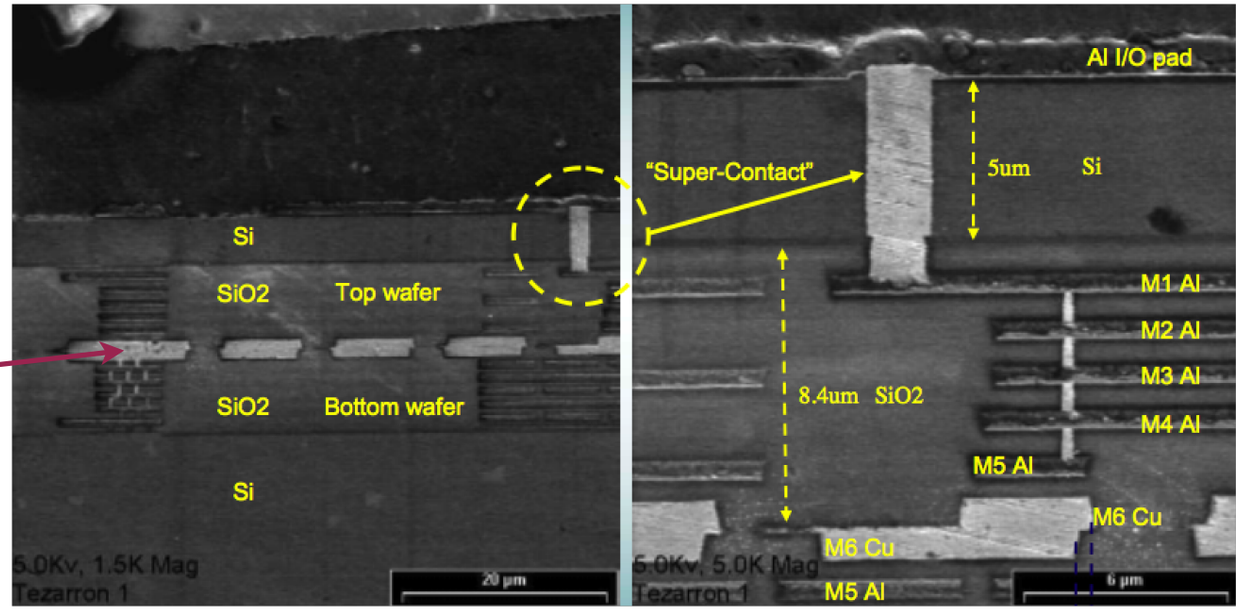
- No fine pitch bump bonds
- Lower capacitance
- Integrated sensors and electronics

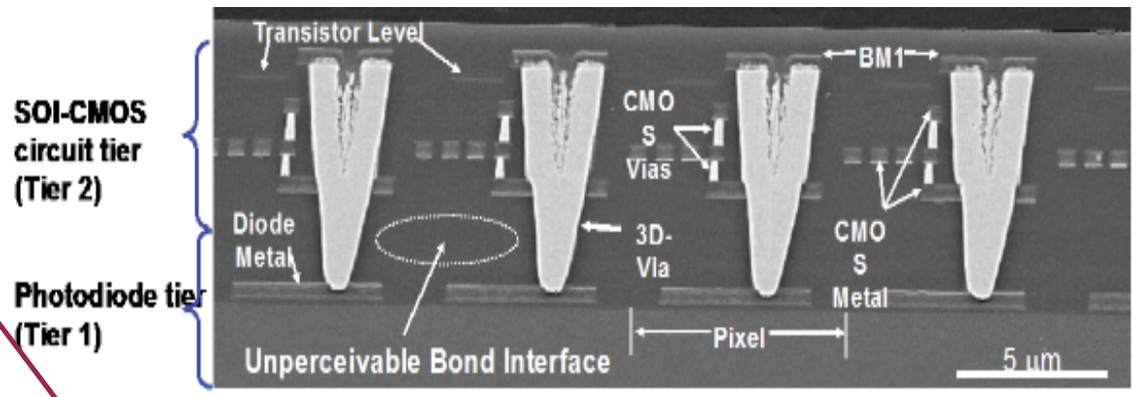


3D Technology

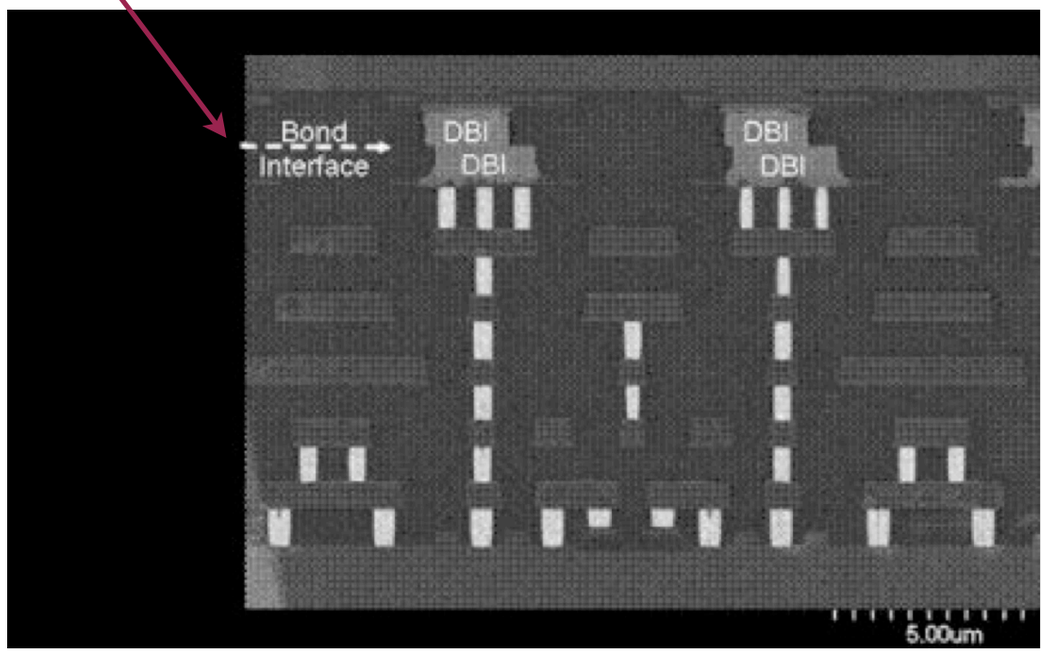
Technology based on:

- **Bonding between layers**
  - **Copper/copper**
  - **Oxide to oxide fusion**
  - **Copper/tin bonding**
  - **Polymer/adhesive bonding**
- **Wafer thinning**
  - **Grinding, lapping, etching, CMP**
- **Through wafer via formation and metalization**
  - **With isolation**
  - **Without isolation (SOI)**
- **High precision alignment**





8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)



3D for HEP

Why is 3D technology important for HEP?

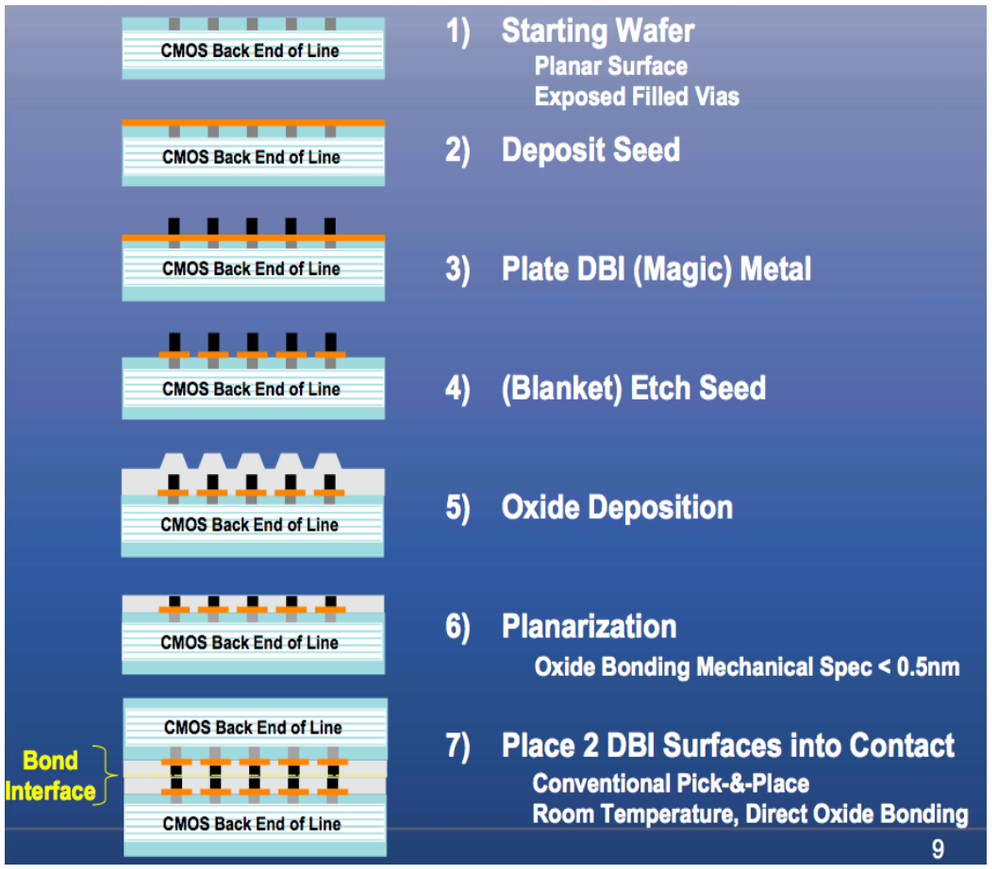
- It enables intimate interconnection between sensors and readout circuits
  - Subpixel readout and control of SiPMs
- It enables unique functionality
  - Digital/analog/ and data comm. tiers
  - Micro/macro pixel designs which can provide high resolution with minimal circuitry
- Wafer thinning enables low mass, high resolution sensors
- Bonding technologies enable very fine pitch, high resolution pixelated devices
- Commercialization of 3D can reduce costs for large areas
- Unique circuit/sensor topologies (CMS track trigger)

Fermilab Initiatives

- ✓ **VIP 3D chip for ILC**
  - **MIT-LL 3D SOI process**
  - **Tezzaron CMOS 3D process**
- **VIPIC chip for x-ray imaging**
- **Thinned detectors**
  - **Laser annealing of the backside contact (with Cornell)**
- **Interconnections**
  - ✓ **DBI bonding of MIT-LL sensors with BTeV readout chip**
  - **Cu-Sn interconnects**
- **Silicon-on-insulator**
  - **Mambo imaging chip with KEK/OKI**
  - **American Semiconductor pixel R&D**
- ✓ **Track trigger for CMS**
  - ✓ **VICTR chip**
- ✓ **Large area arrays with active tiles**

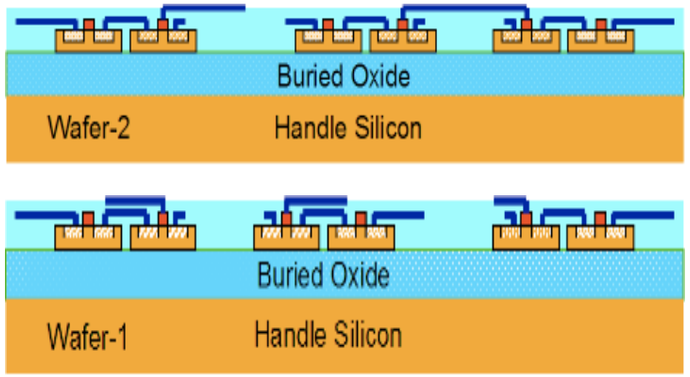
Processes Explored

Ziptronix Oxide Bonding

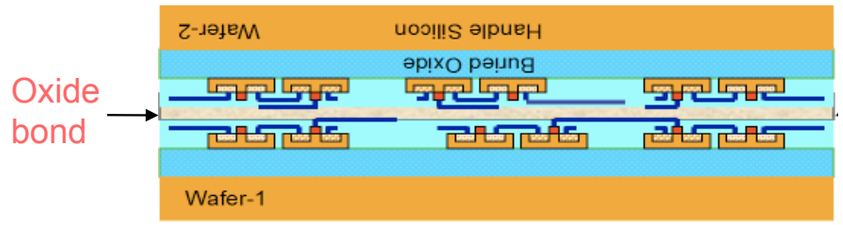


MIT-LL Oxide wafer bonding

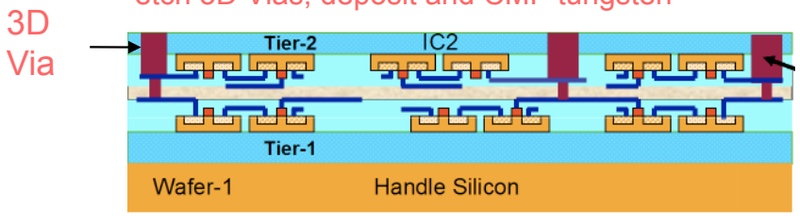
1) Fabricate individual tiers

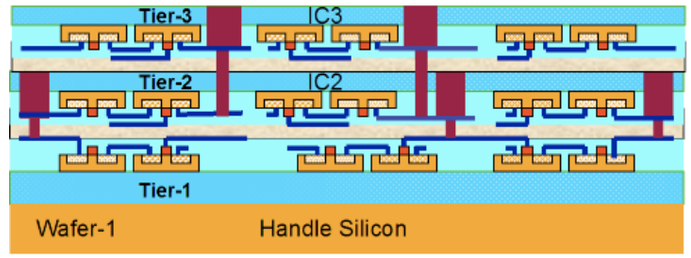


2) Invert, align, and bond wafer 2 to wafer 1

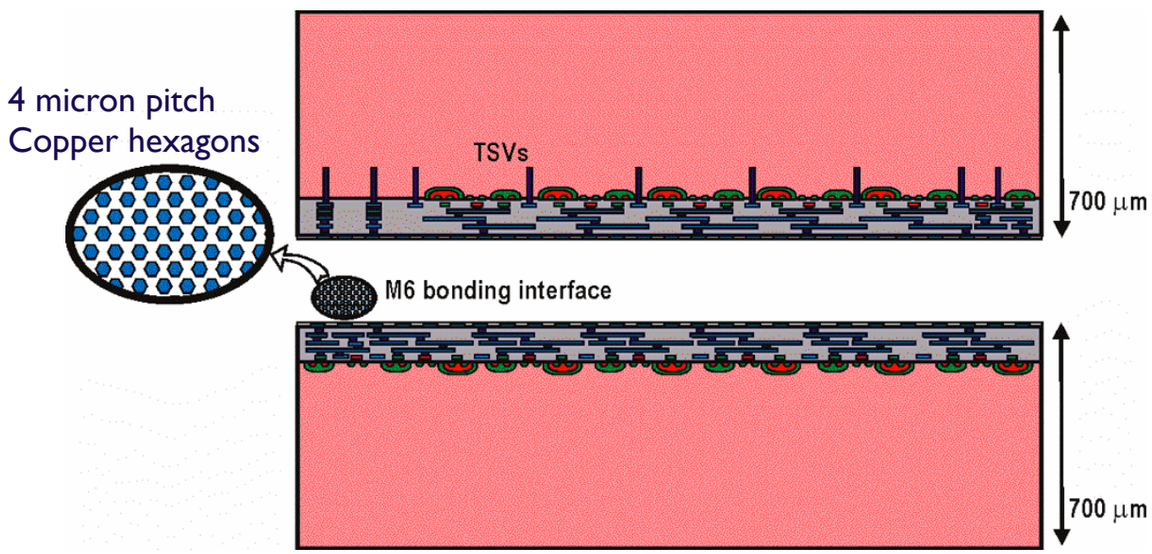


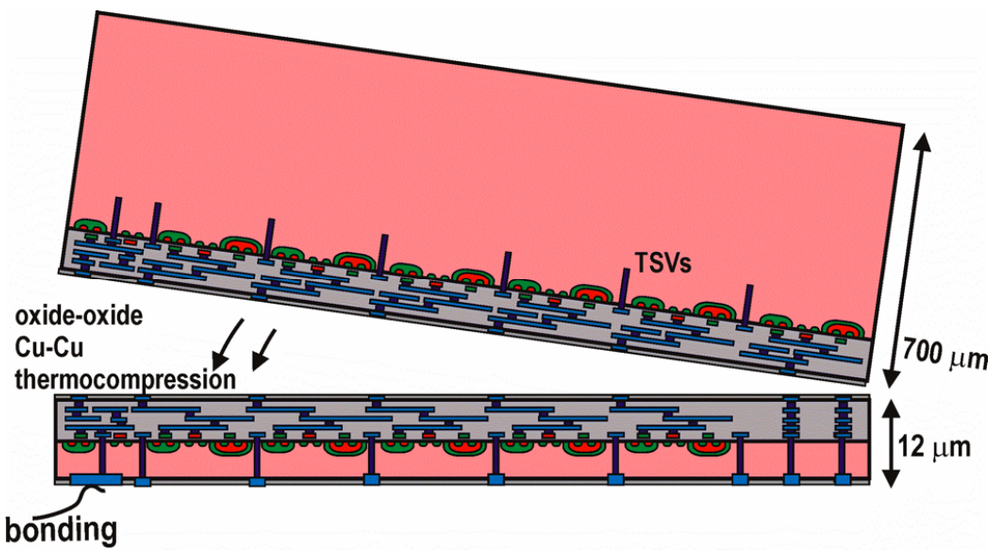
3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten





Tezzaron cu-cu bonding

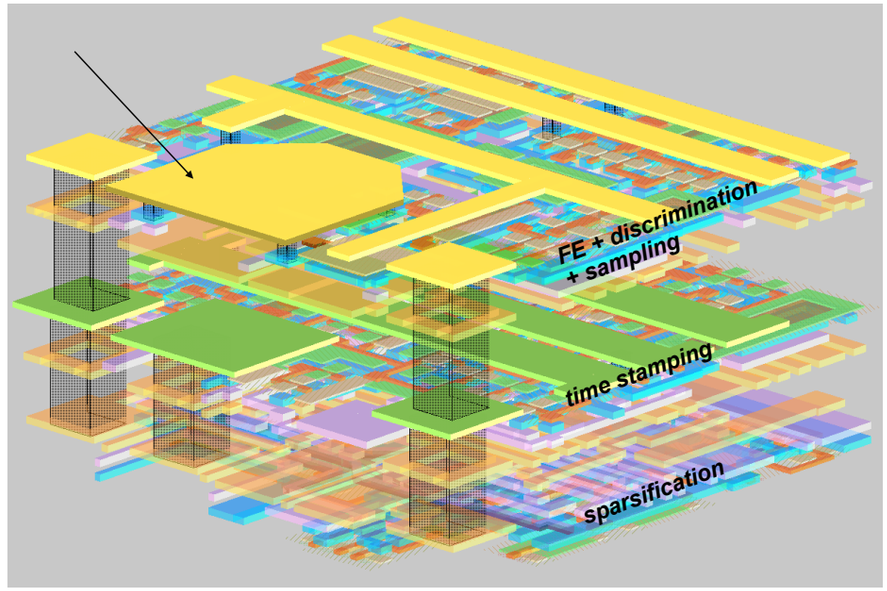


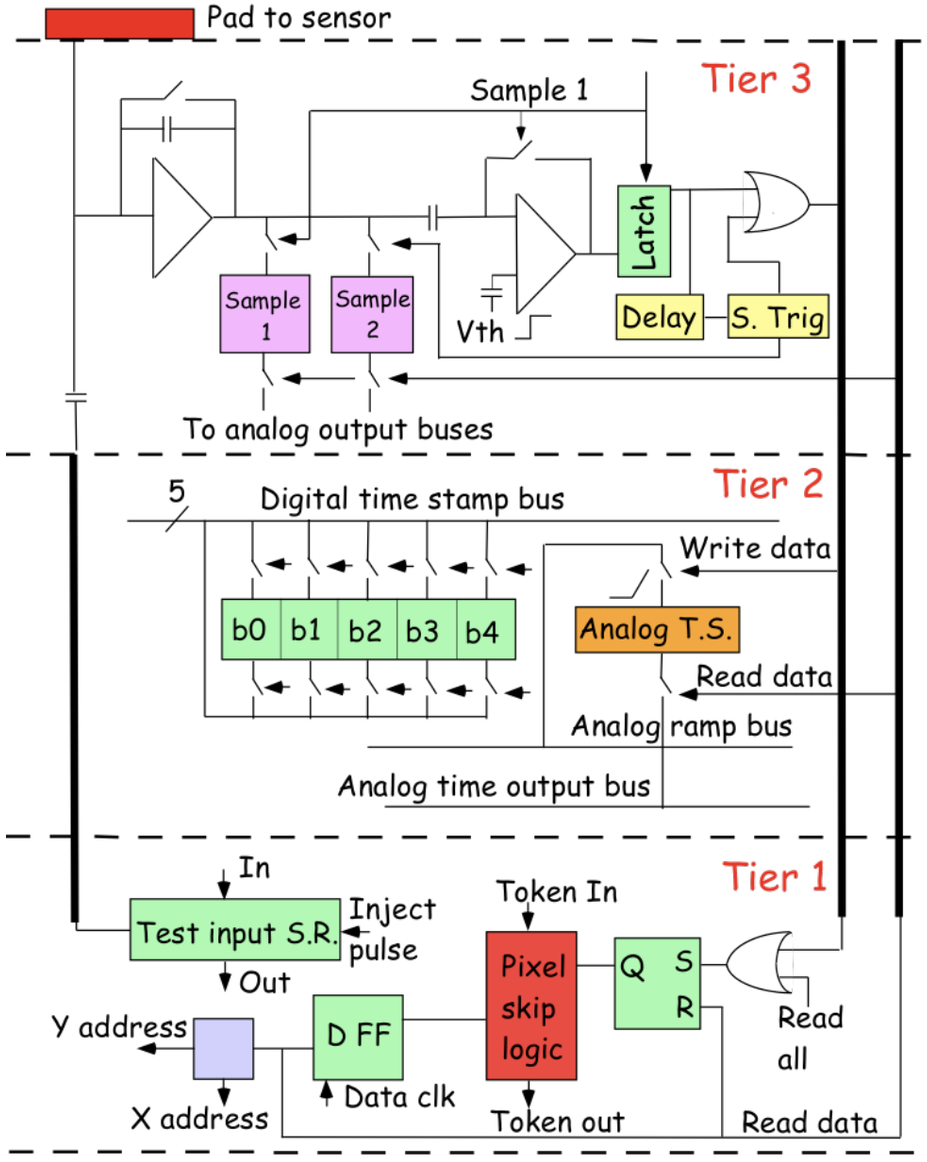


3D Chip for ILC Vertex

Goal - demonstrate ability to implement a complex pixel design with all required ILC properties in a 20 micron square pixel

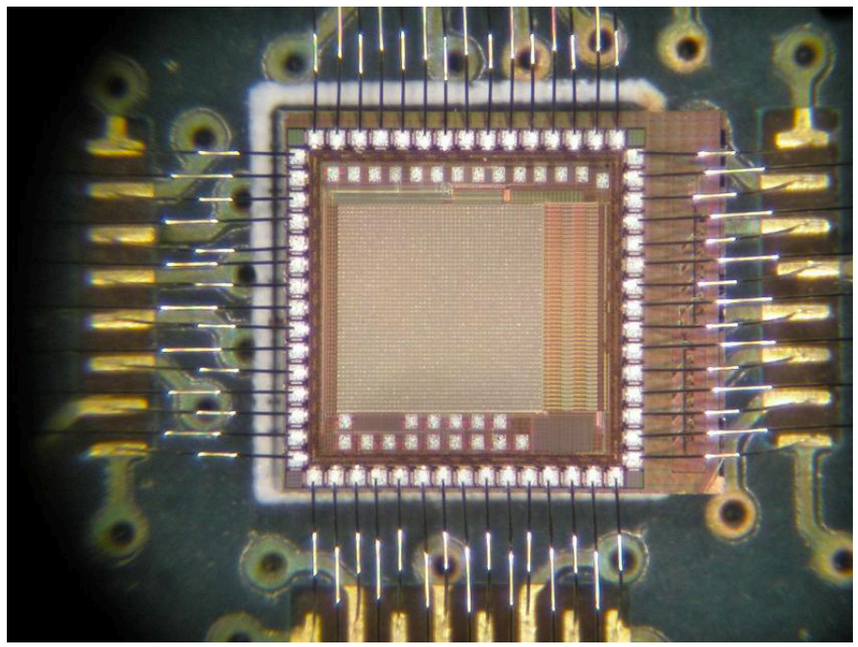
- Previous technologies limited to very simple circuitry or large pixels
- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
- 3D density allows analog pulse height, sparse readout, high resolution time stamp in a 20 micron pitch pixel.
  - Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
  - 64 x 64 pixel demonstrator version of 1k x 1k array.
- Submitted to 3 tier DARPA-sponsored multi project runs.
- Slow power front end 1875 µW/mm2 x Duty Factor
- Work completed in 2010

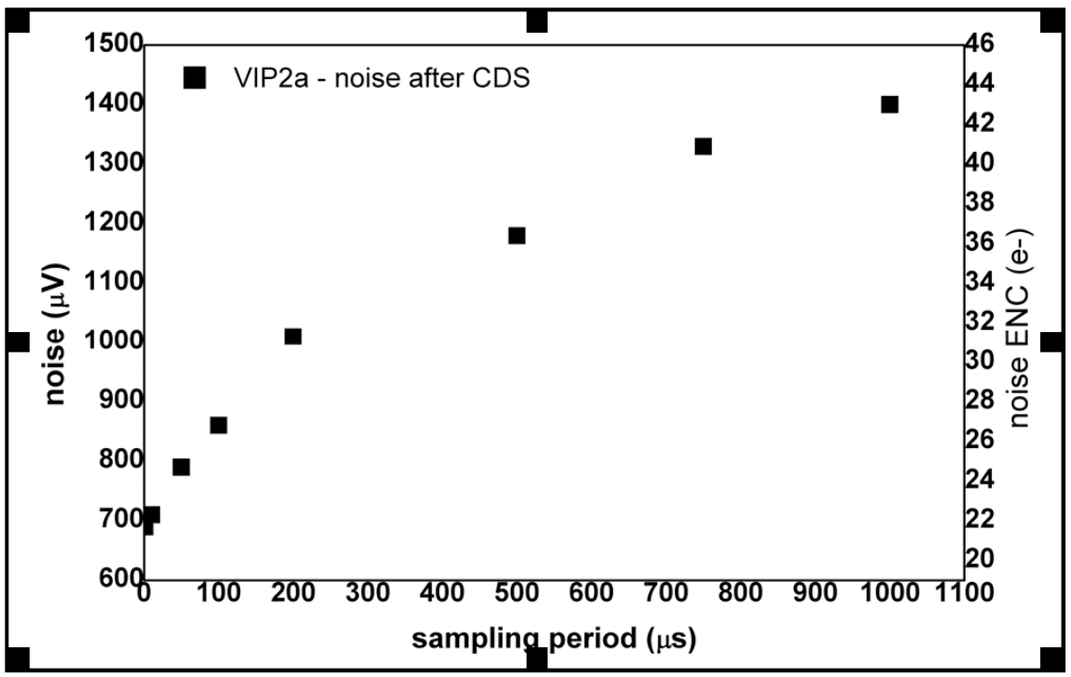


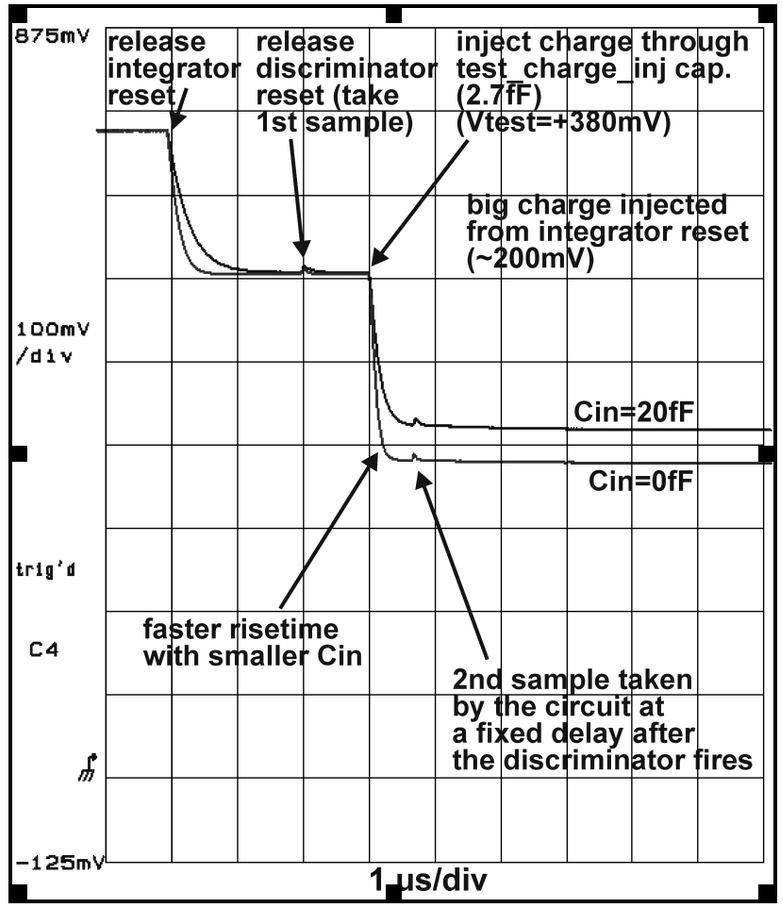


VIP Test Results

- Good noise performance (20 fF simulated load, DCS with differential analog output, 1 us sample time, Tr=120 ns, Ib=0.5uA, Cs=100fF)
- Gain ~ 200 mV/fc at CL = 20 fF
-



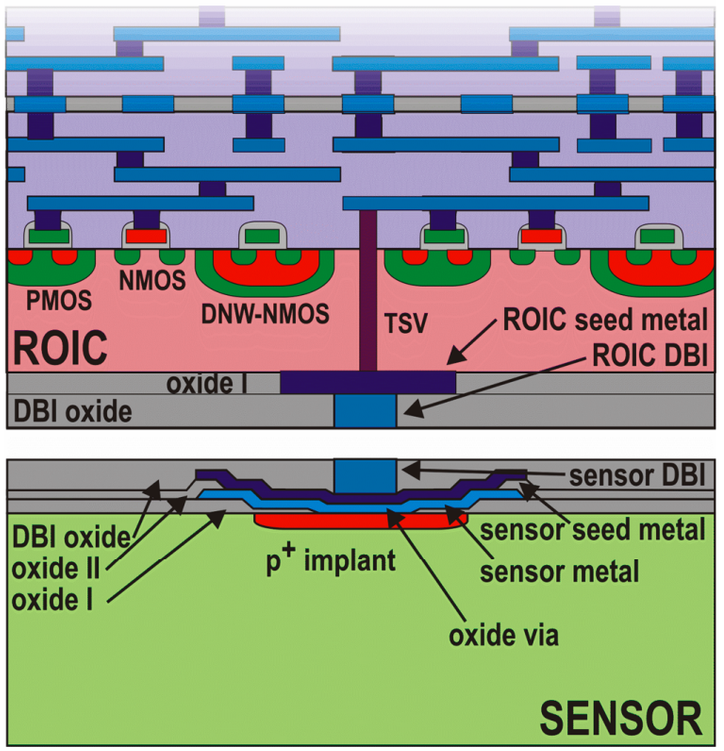


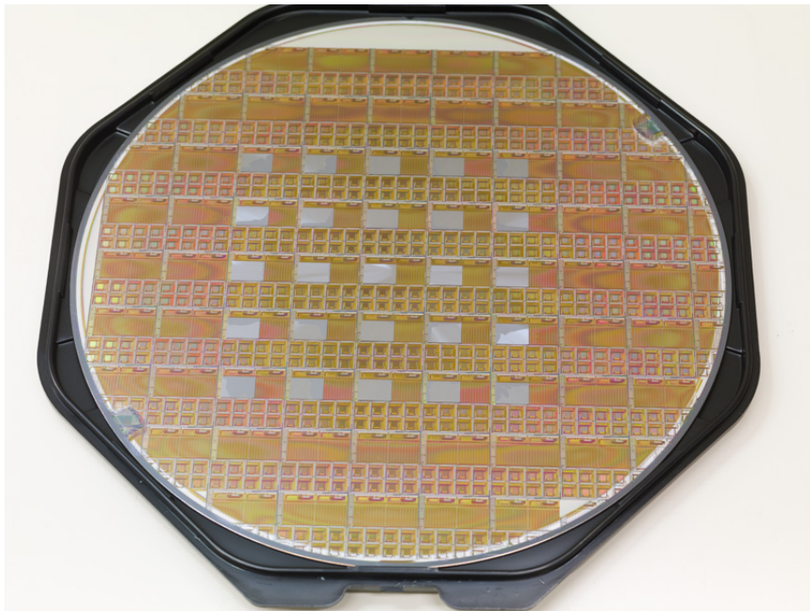


Oxide Bonded Sensors and Chips

- Ziptronix Direct Bonded Interconnect (DBI) based on formation of oxide bonds between activated SiO_2 surfaces with integrated metal
  - Silicon oxide/oxide initial bond at room temp. (strengthens with 350 deg cure)
  - Replaces bump bonding
  - Chip to wafer or wafer to wafer process
  - Creates a solid piece of material that allows bonded wafers to be aggressively thinned
  - ROICs can be placed onto sensor wafers with 10 μm gaps - full coverage detector planes
  - ROICs can be placed with automated pick and place machines before thermal processing - much simpler than the thermal cycle needed by solder bumps

Process was developed to allow 3D electronics integration of ICs by thinning to imbedded through silicon vias after bonding

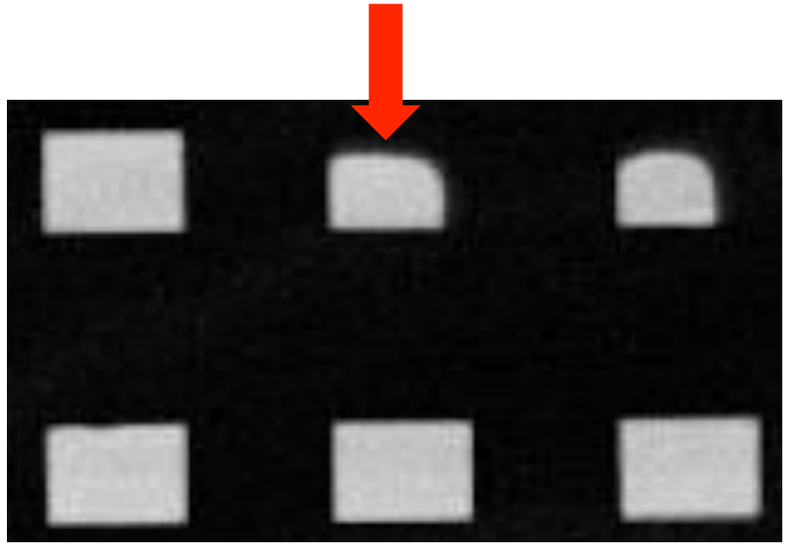




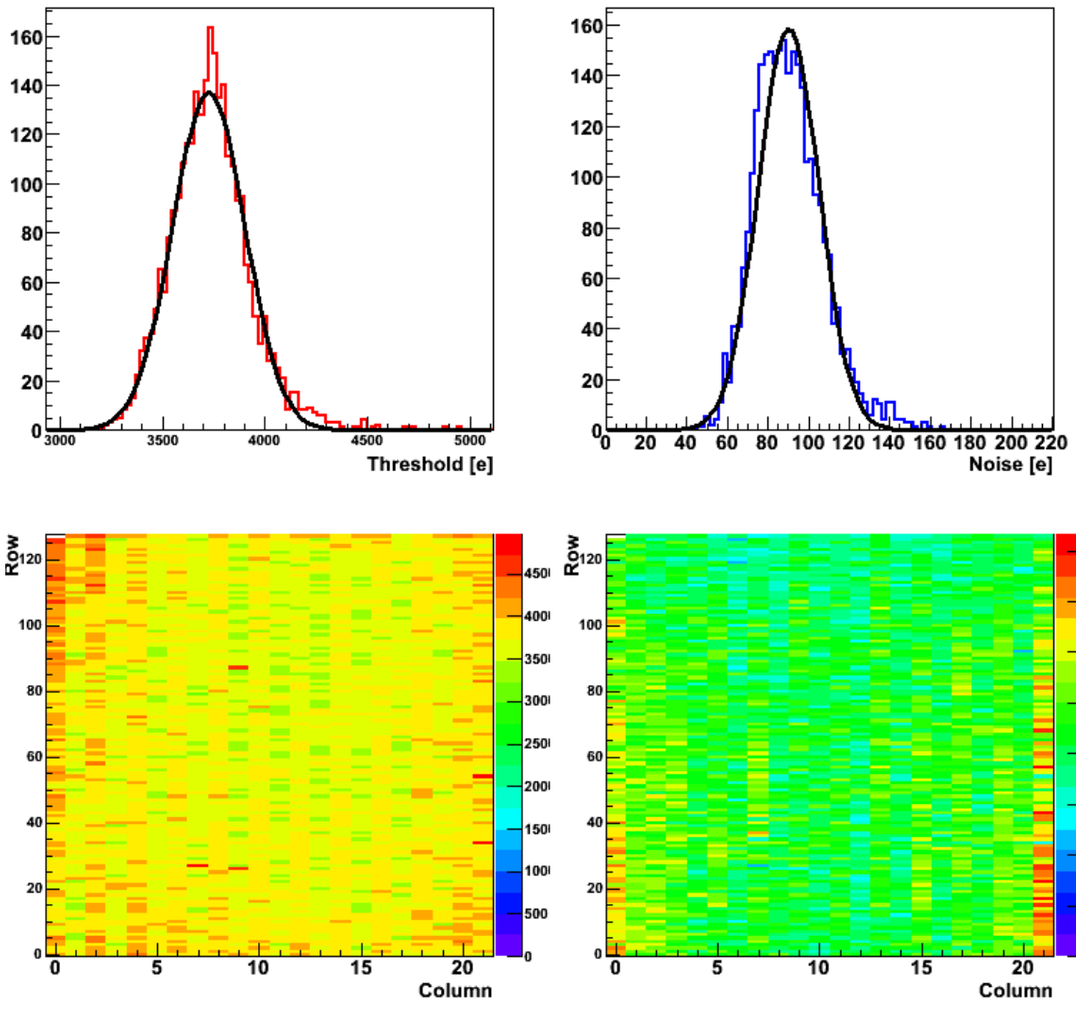
Sensors bonded to FPIX wafer

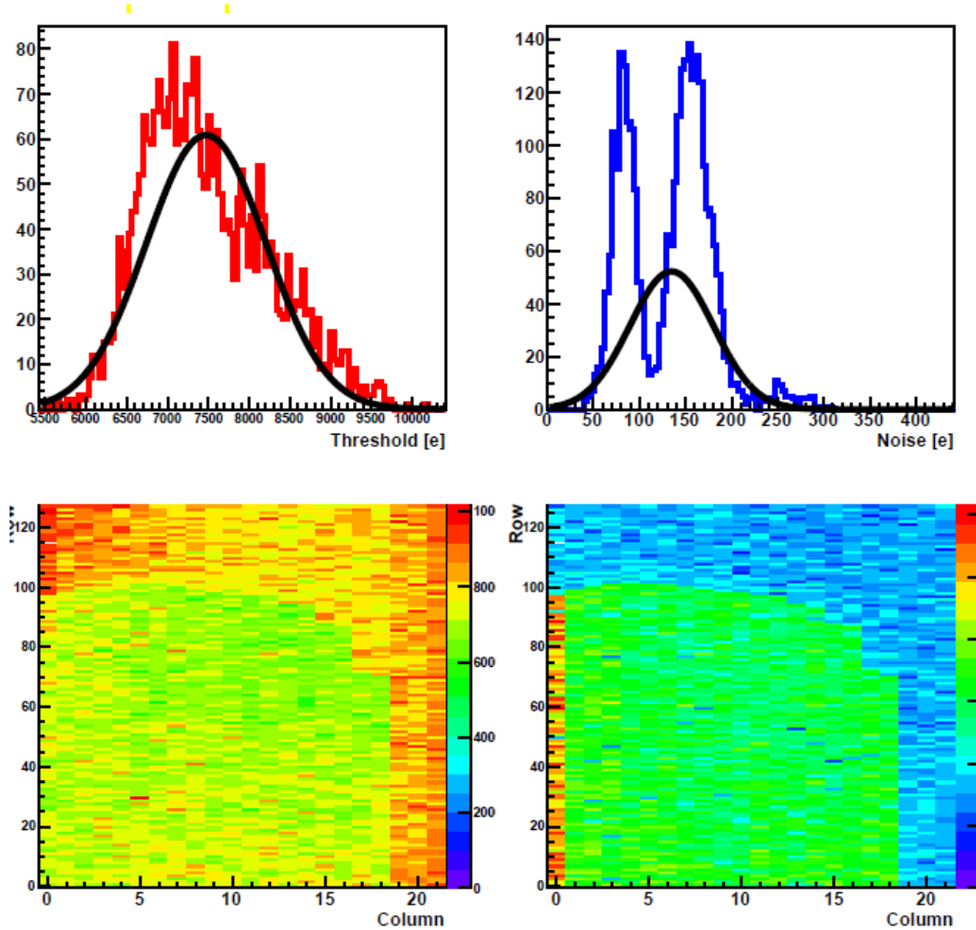
Bonded Device Tests

- 100% bonded channels in chips with good acoustic micro. scan
- process does not add noise
- radiation hard



Example of a die with a void in the oxide





(Z.Ye)

CMS Track Trigger

How can we Maintain and Extend the physics capabilities of CMS after 10 years of operation at LHC?

Upgrades to the LHC beyond 2020 will emphasize luminosity

- $5x10^{34}$ at 25 or 50 ns bunch spacing
- As many as 200 interactions per crossing

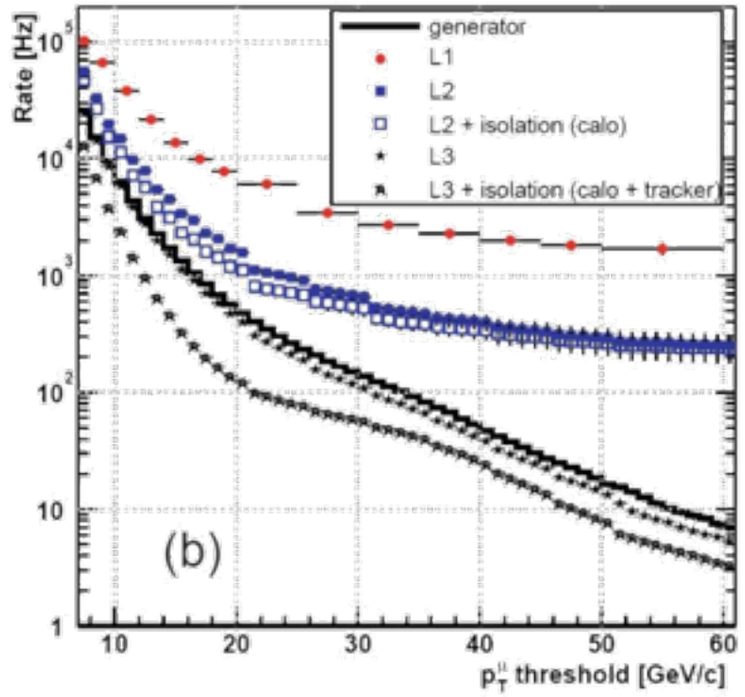
We *may* need to be sensitive to very small cross sections to select new physics signatures.

We *will* need to cope with 100's of interactions per crossing

The trigger is the tool we use to select physics events - how can we maintain and extend it into the 2020s?

CMS Trigger at High Luminosity

Use of Tracker input to Level-1 trigger



- μ, e and jet rates would exceed 100 kHz at high luminosity
- Increasing thresholds would affect physics performance
- Performance of algorithms degrades with increasing pile-up
- Muons have increased background rates from accidental coincidences
- Electrons/photons: reduced QCD rejection at fixed efficiency from isolation
- Add tracking information at Level-1

Full-scope objectives:

- Reconstruct "all" tracks above 2 - 2.5 GeV
- Identify the origin along the beam axis with ~ 1 mm precision

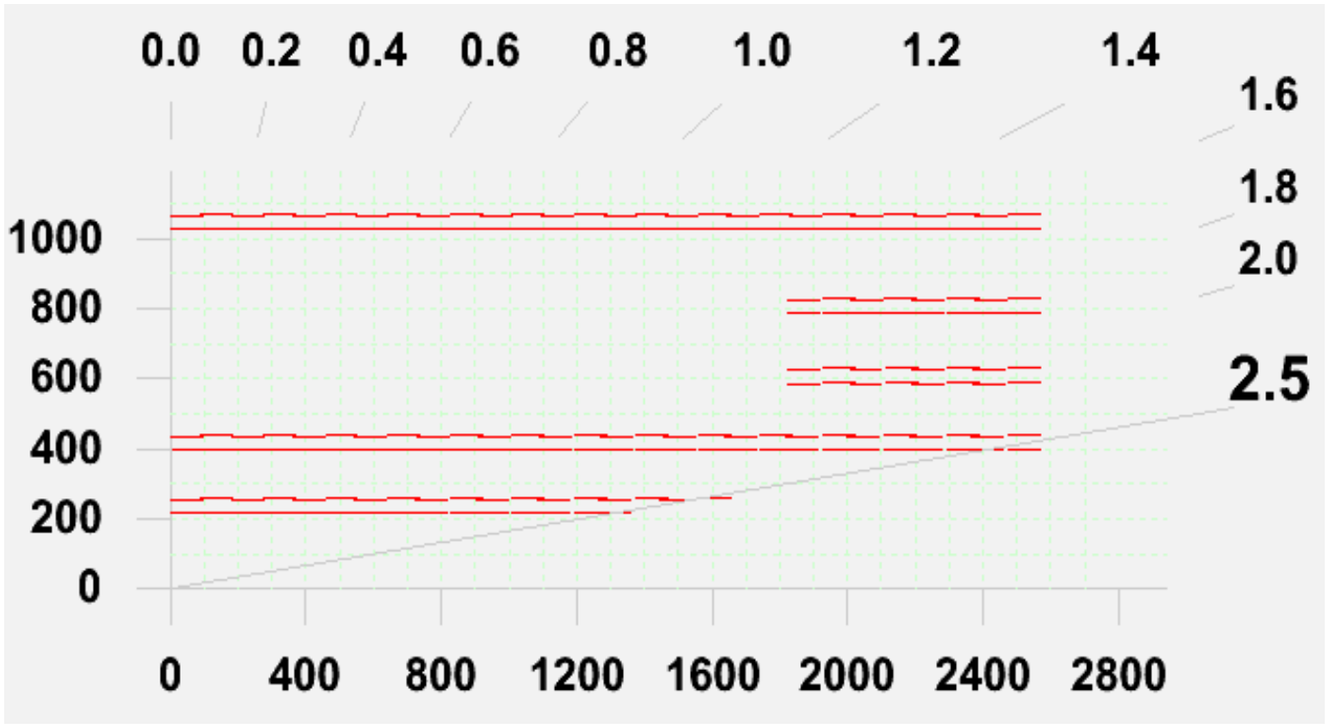
How Can we build a track trigger at Level 1?

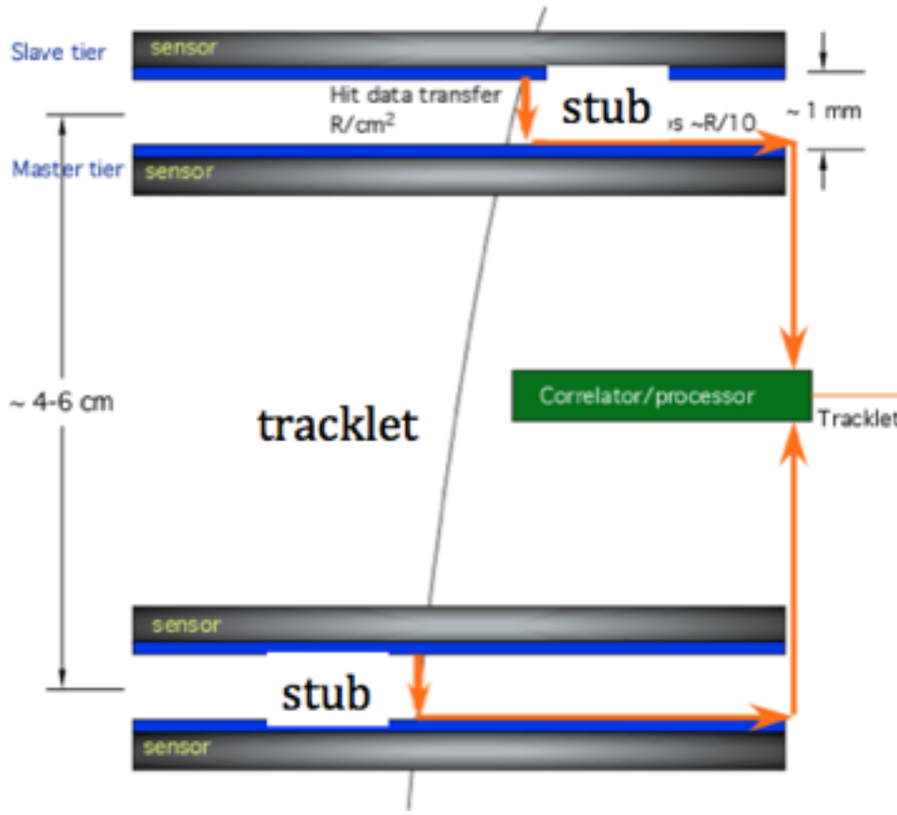
Must be (40MHz/100kHz)=400 times faster than a L2 trigger like FTK or SVT .This is especially hard for a silicon-based tracker with potentially huge data volumes

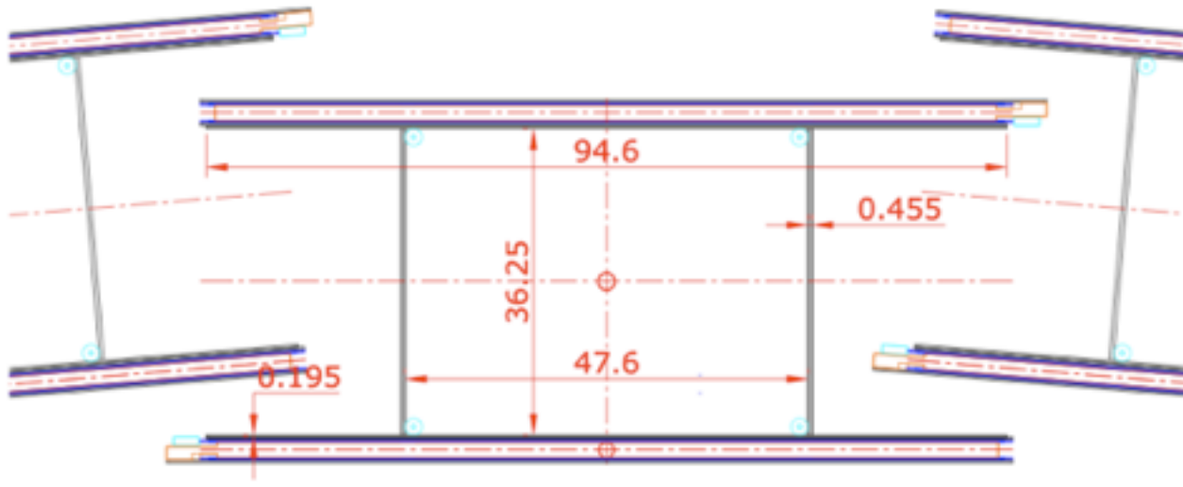
Principles:

- The trigger must be designed into the tracker geometry from the start
- Good Z resolution to reduce background event candidates. Minimize the tracks used for isolation.
- Design the system geometry so all operations are "local" - minimize data transmission. Use hierarchical design to limit overall data flow
- Limit rate at the front end by using correlated layers (x20 rate reduction)

Tracker Design







Stubs found in sensor pairs

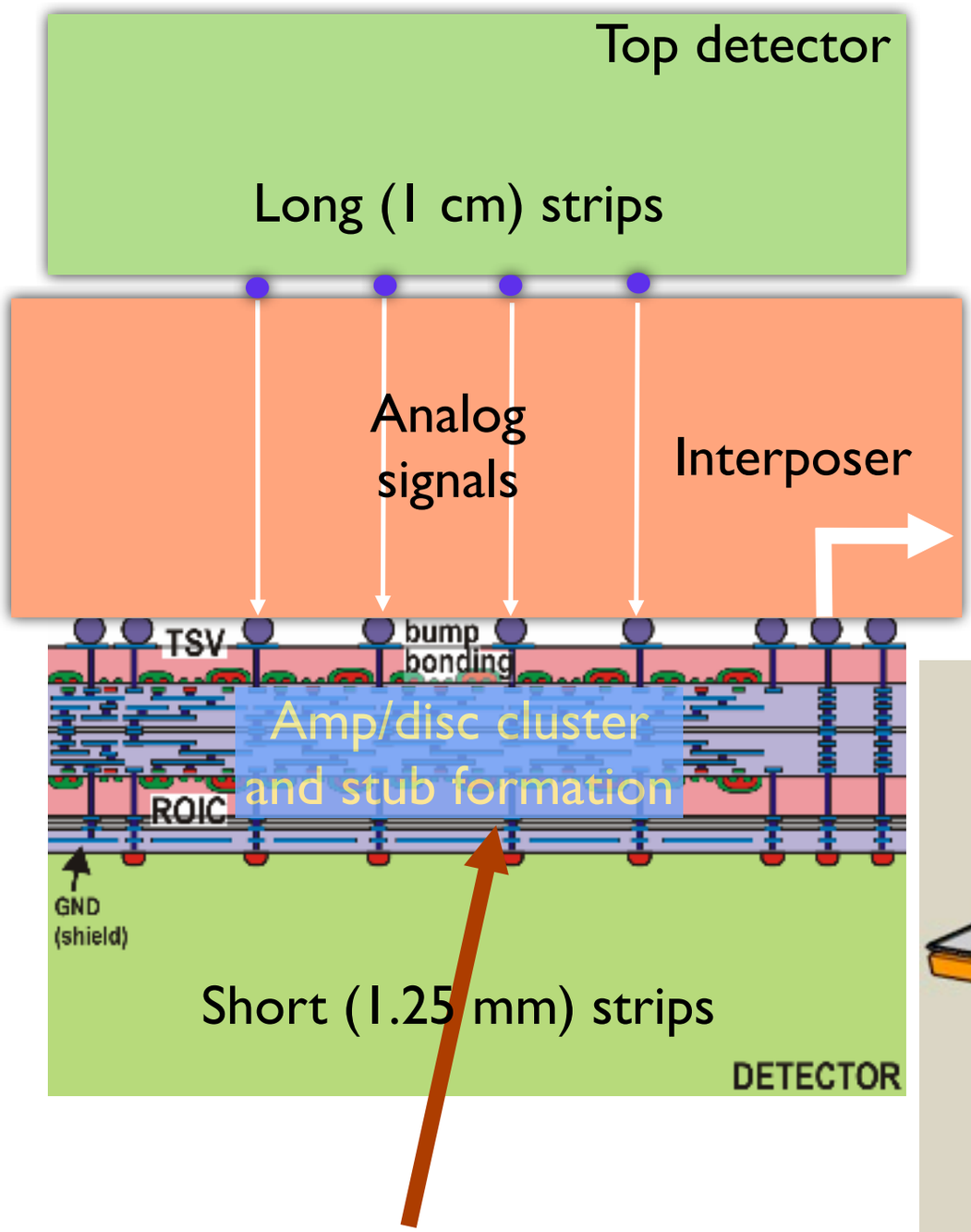
- 2.5 GeV threshold
- 3D chip used to correlate top and bottom sensors

Tracklets found in module pairs in a rod

- Overlap designed to limit tracklet search to single rod

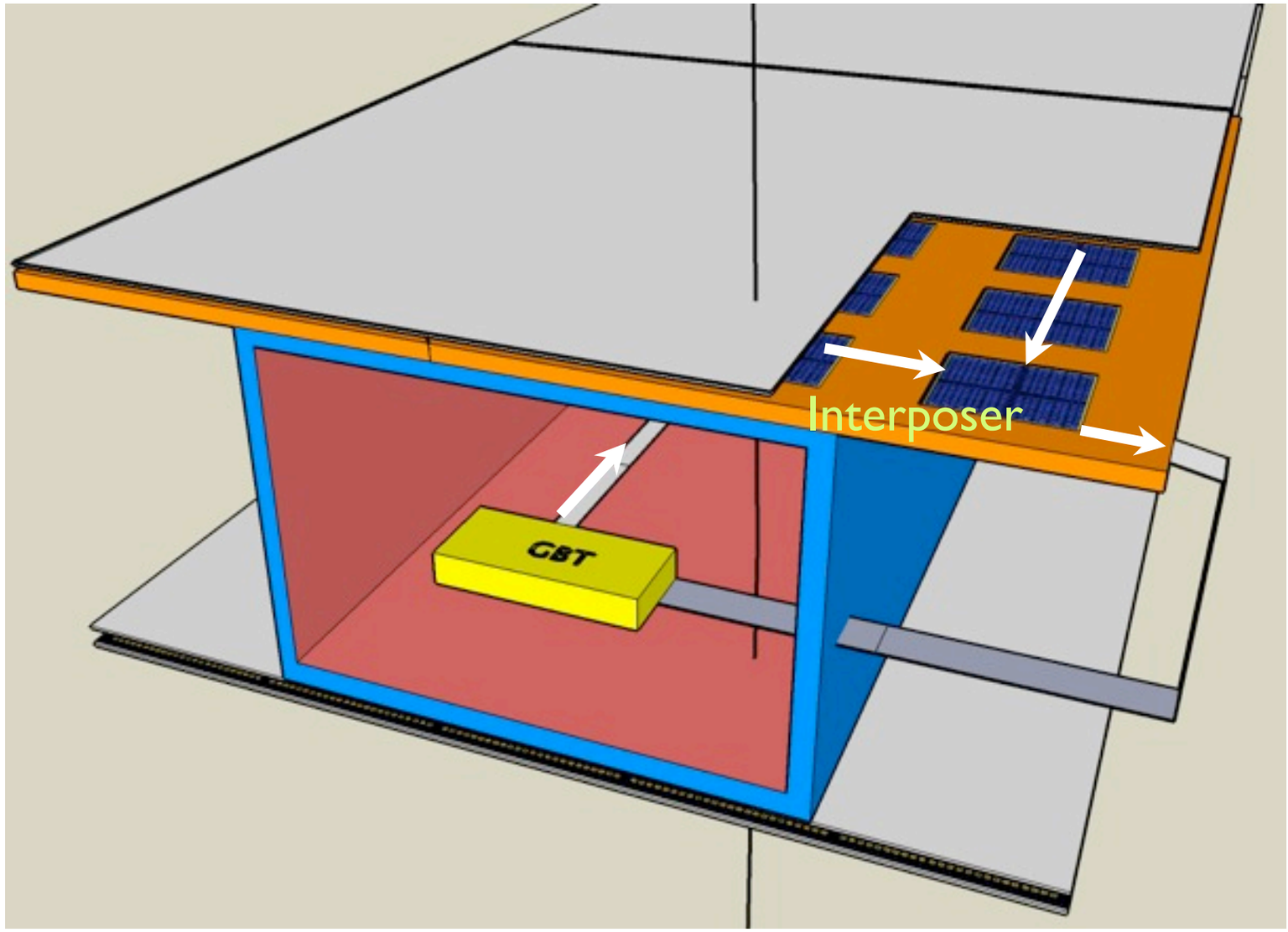
Tracks found using precise extrapolation of tracklets to other layers (tracklets have good Pt, position resolution)

3D Module Data Flow



ROIC sees signals from top and bottom sensors all correlations local

Top sensor analog information flows through interposer to IC mounted on bottom
Long strips on top provide r-phi minimize number of interposer connections
Short strips on the bottom provide Z resolution
ROIC amplifies and discriminates forms stubs and manages pipeline



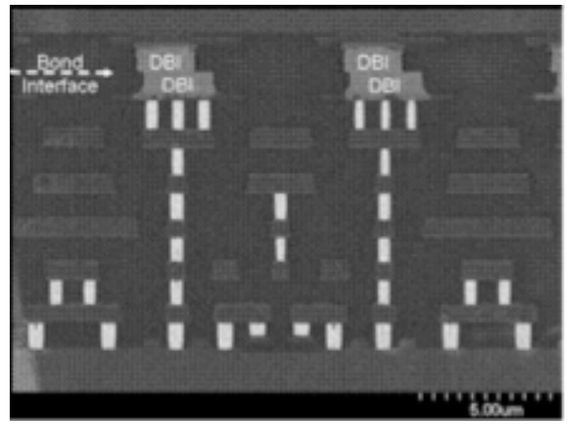
Why 3D for Track Trigger?

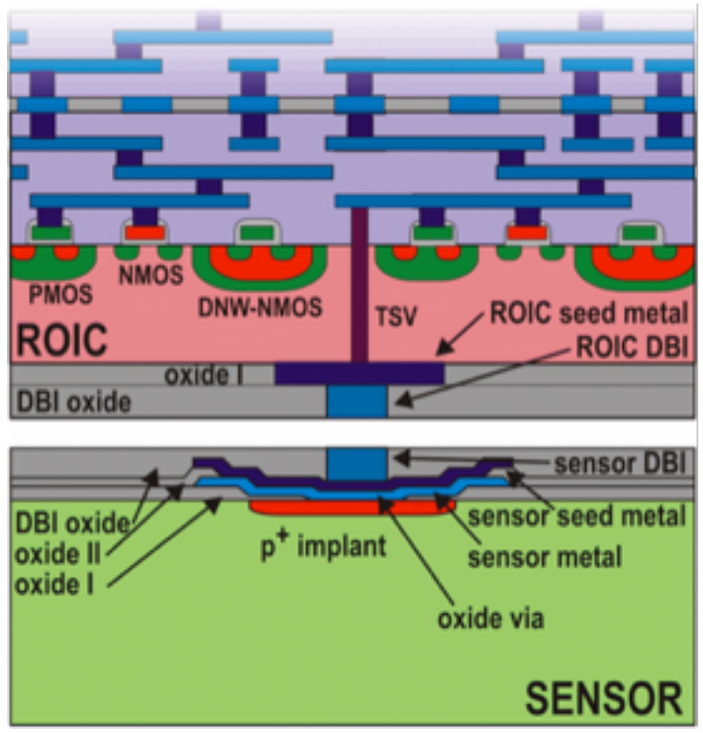
A variety of 3D technologies allow direct contact to a sensor both above and below the readout chip

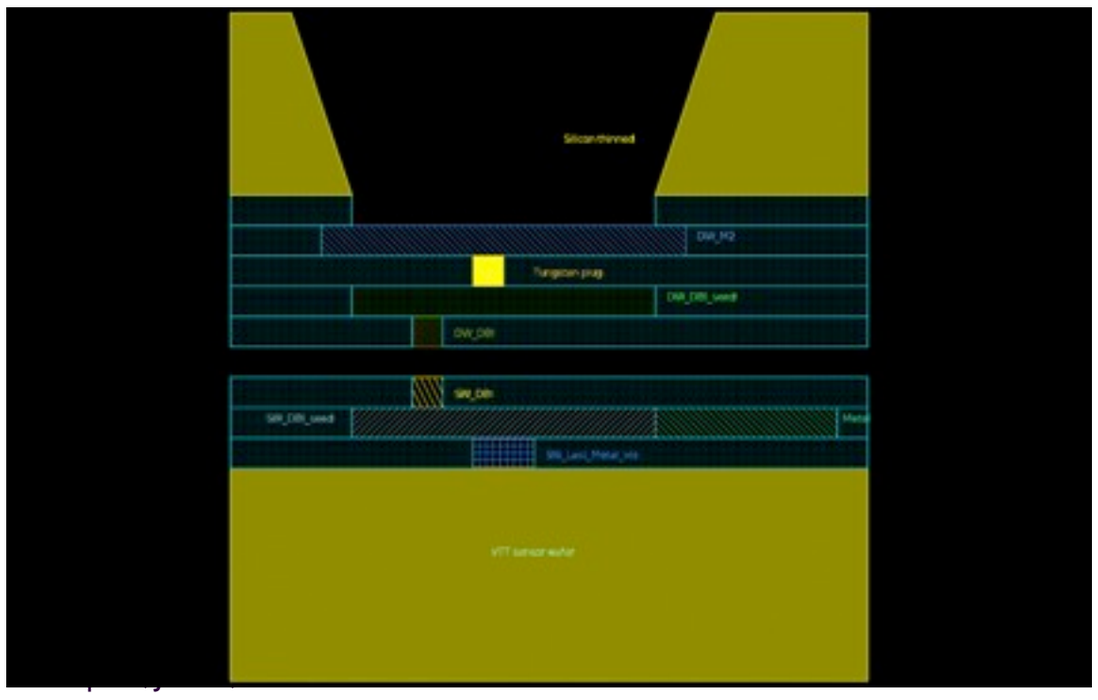
Backside connections mean no area is lost to wirebond pads - this enables large modules with minimal dead area

Possible technologies

- Silicon-on-insulator with detector in "handle"
- Lepix type CMOS with high resistivity substrates
- ✓ CMOS with through-silicon-vias oxide bonded to sensor - fab support, rad hard, scalable to large volumes
- "Via Last" interconnects fabricated on finished CMOS wafers
- ✓ Readout bonded to sensor thinned, and pad contacts exposed

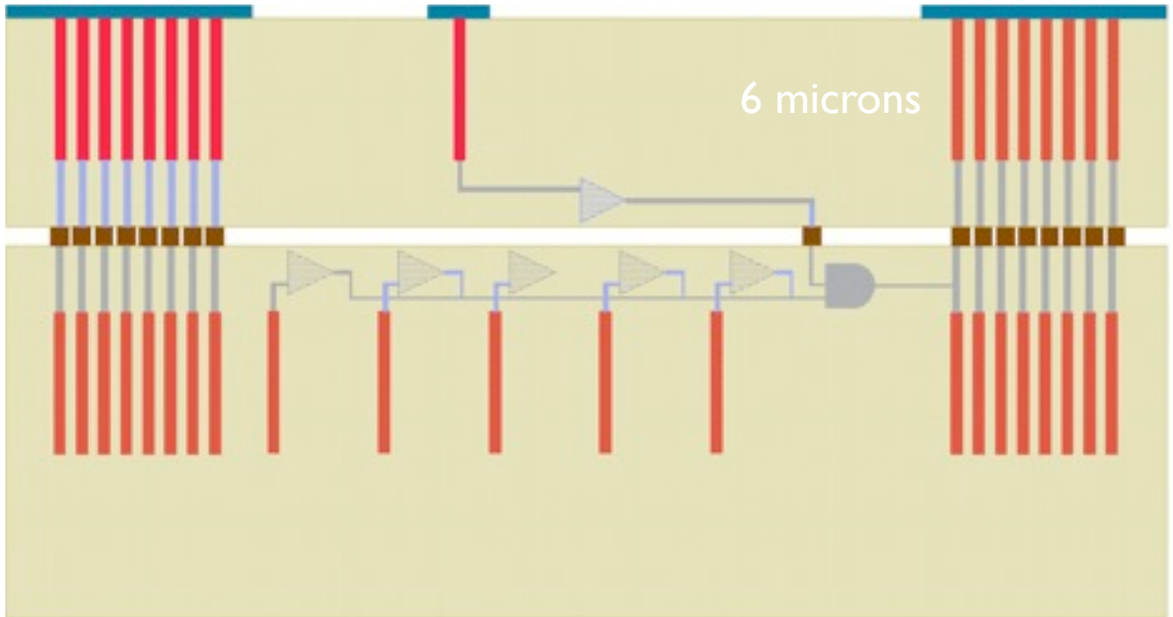






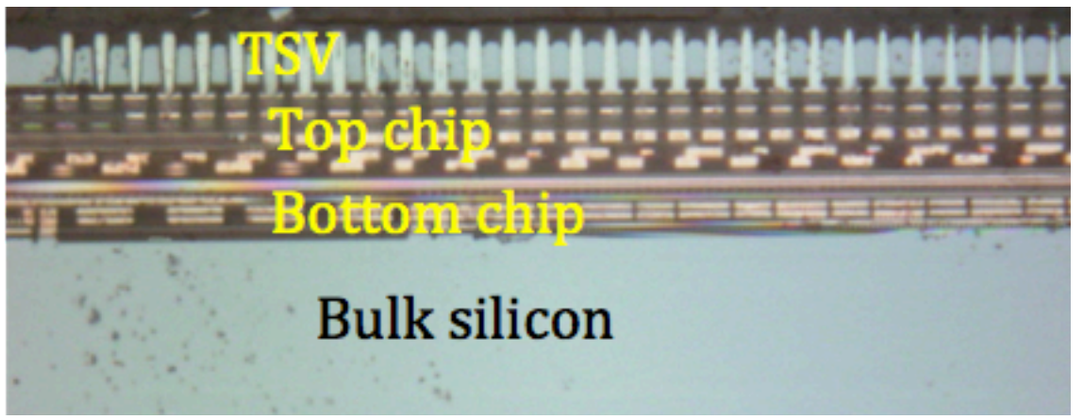
Top wafer is etched away in this region to expose "bottom" of pads

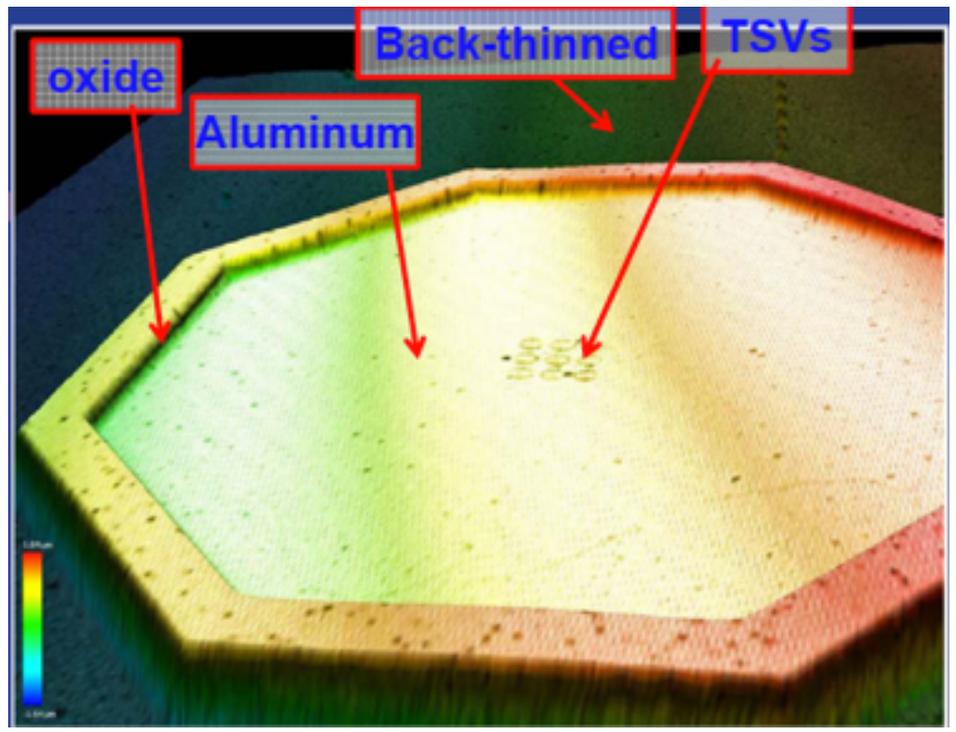
VICTR 3D Chip



The VICTR chip is designed to demonstrate the principles of a track trigger sensor/ROIC

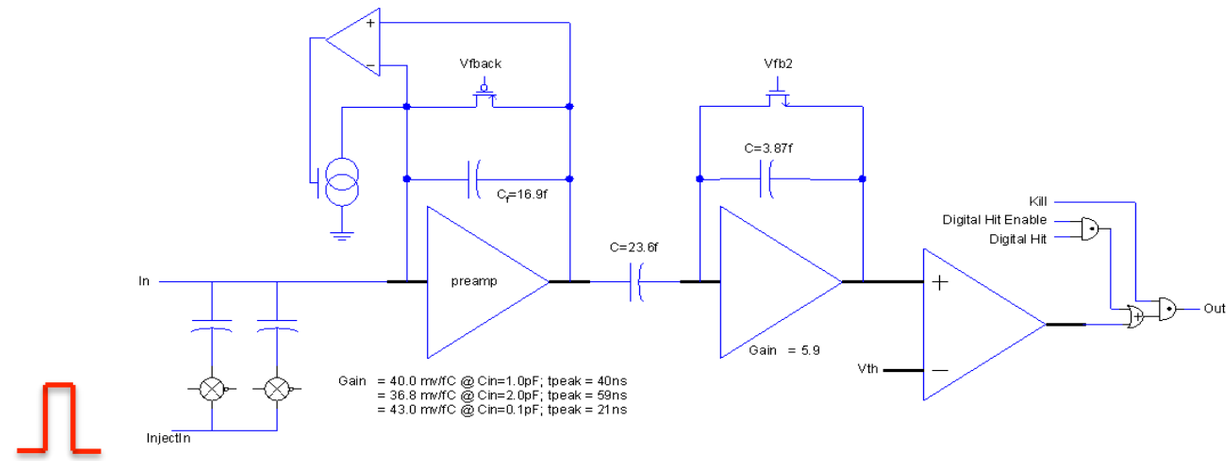
- Part of Fermilab 3DIC run
- Modified FEI4 (Atlas) front end
- First chips delivered last Sept had alignment problems but all processes needed for CMS worked well.
  - backside thinning
  - TSV contact
  - Backside metalization

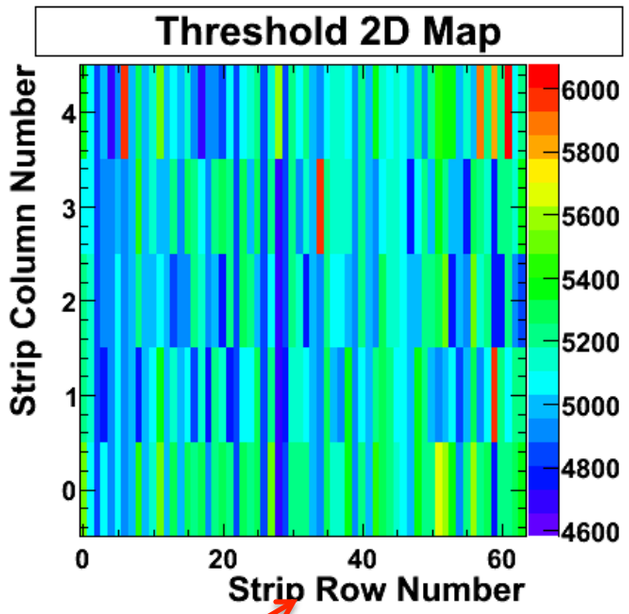


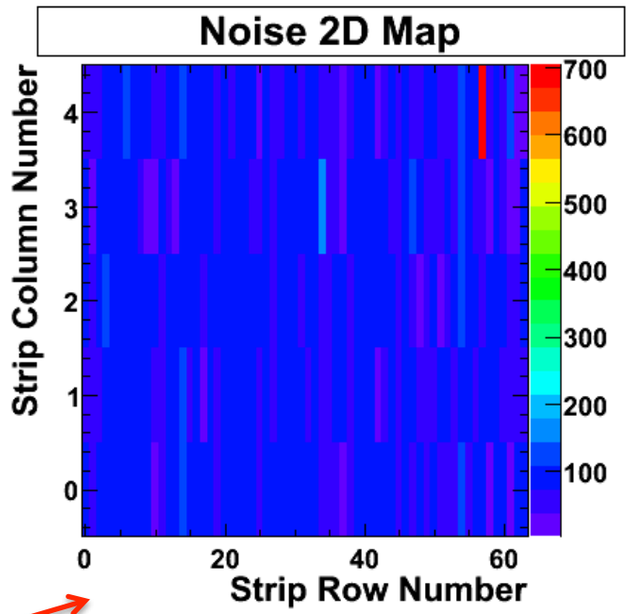


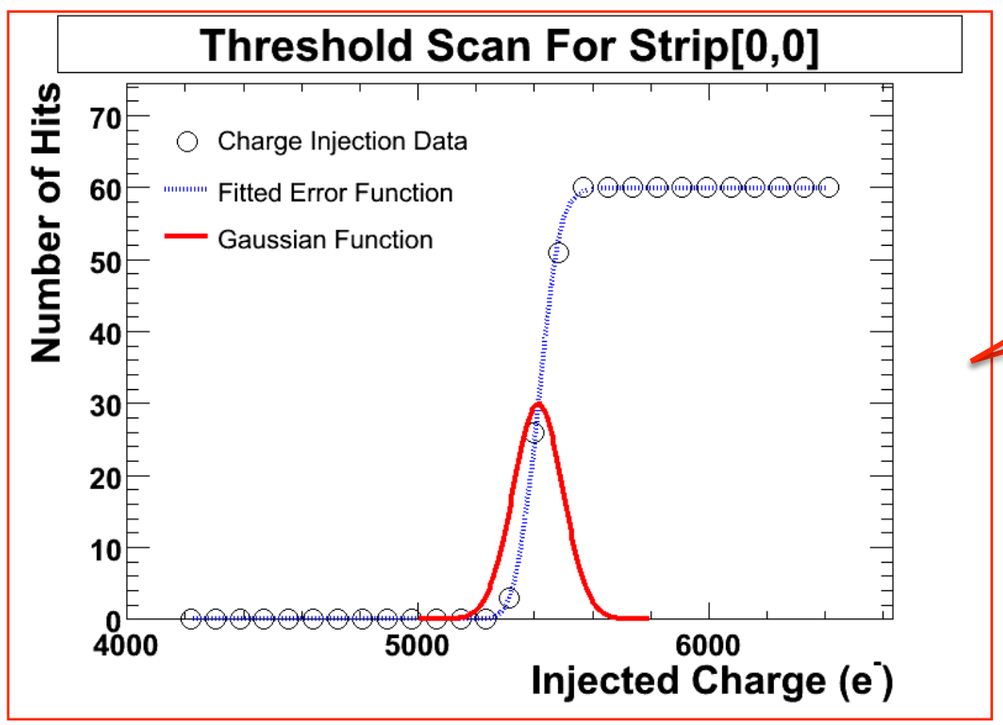
VICTR Test Results

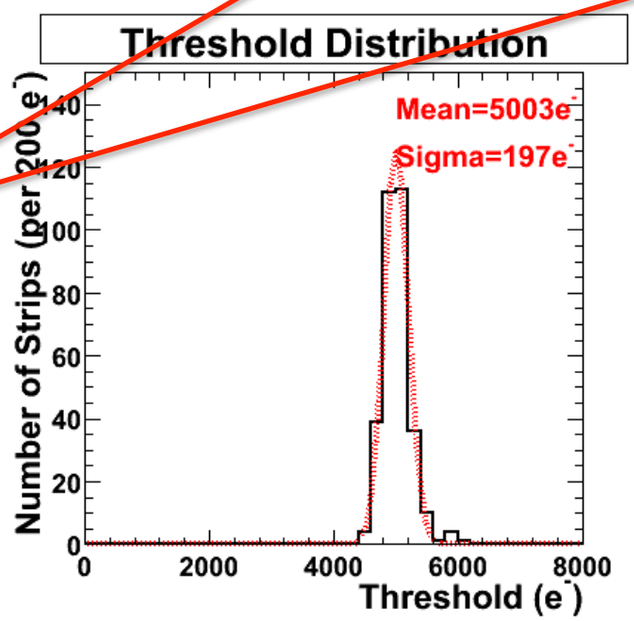
- Tests using NI flex rio systems
- Good threshold tuning and noise performance

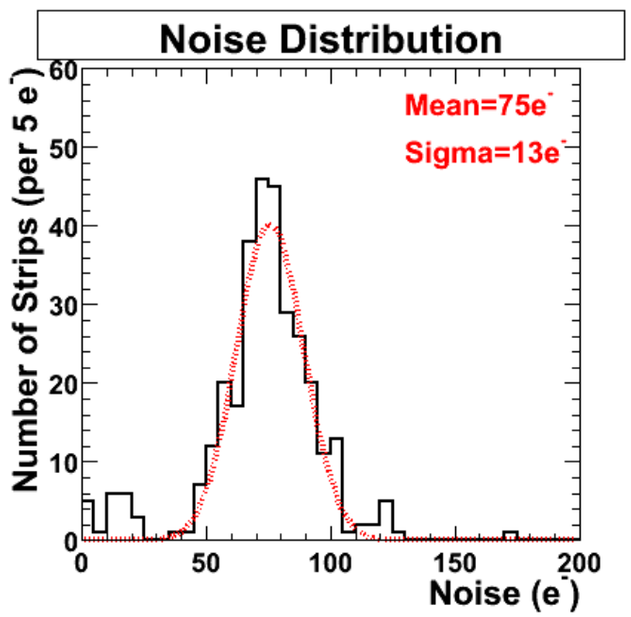












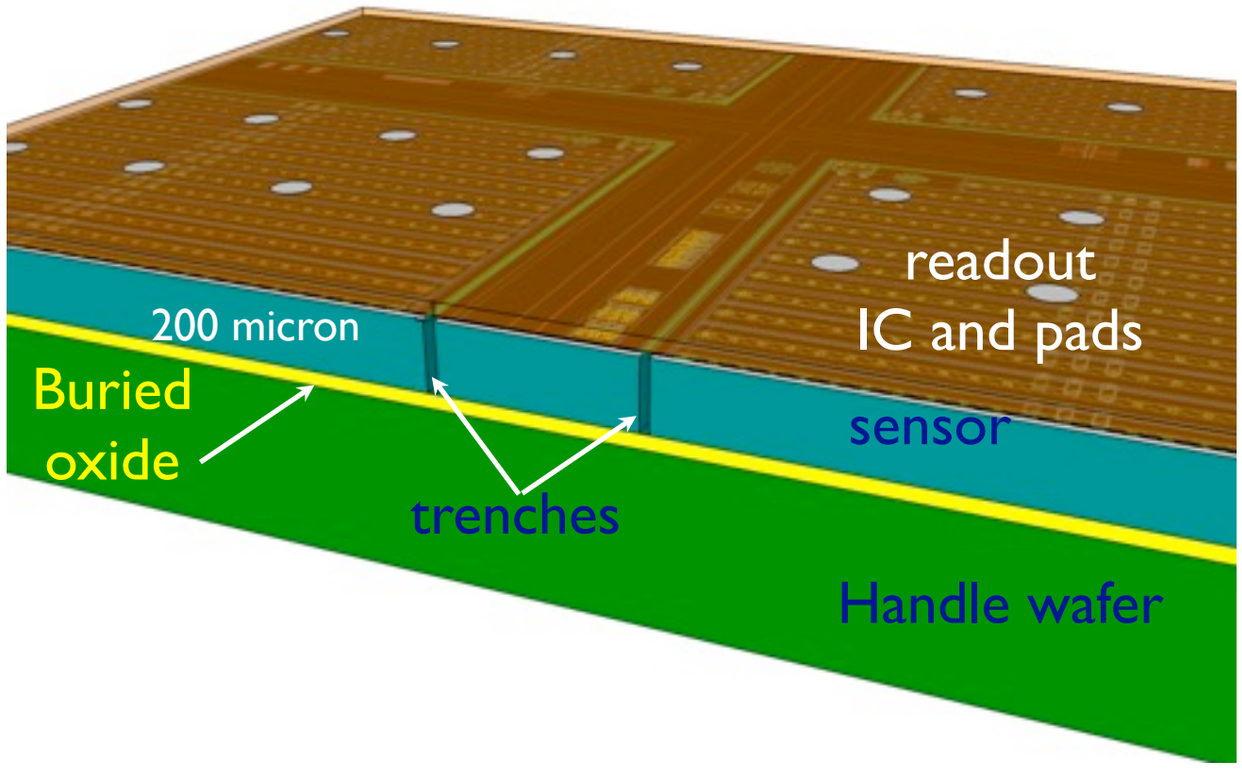
Tiling Pixelated Sensors

The greatest risk in the Long barrel/3D concept are cost and yield issues for large area arrays of pixelated sensors

- The costs are not intrinsic to CMOS technology - CMOS wafers are \$3/cm^2 vs \$10/cm^2 for Hamamatsu
- There is a "placement yield" for the bonding process which may be 80-90%
- For a large module with 25 sensors this gives an unacceptable yield.

To solve this we are exploring active edge "tiles" of sensors integrated with readout chips

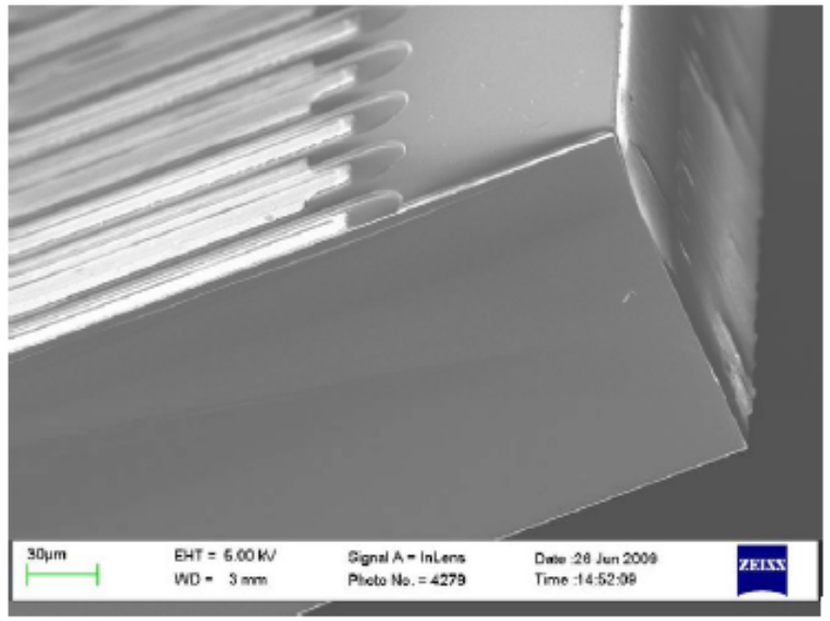
- Fine pitch sensor-readout bonding would use the oxide/DBI process
- Active edges would provide reticule-sized tiles
- Coarse pitch (~1 mm) bonding of the tiles to the interposer using cheap, reworkable technology



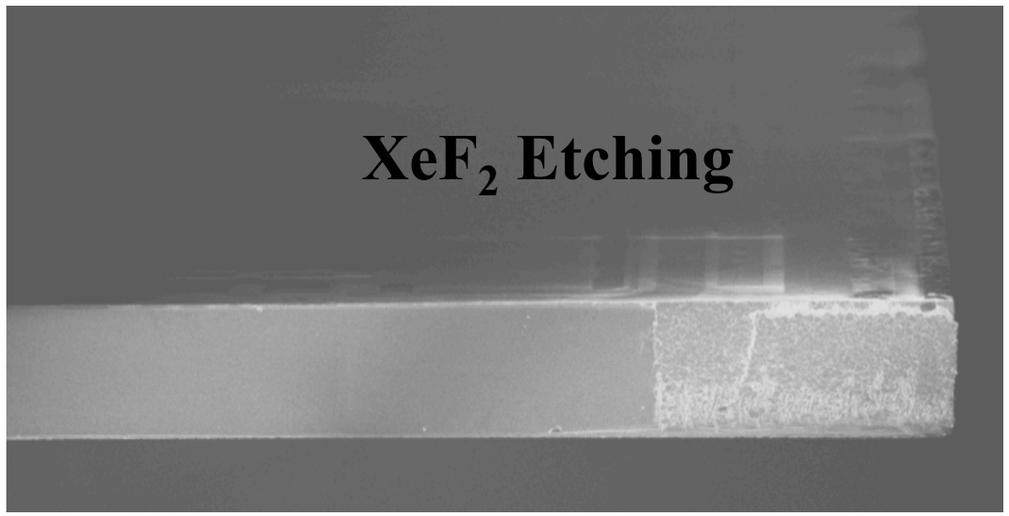
Active Edge Sensors

An outgrowth of 3D detector development by Sherwood Parker and collaborators

- Deep reactive ion etch of silicon to create a nearly vertical trench with smooth edges avoids charge generation centers
- Filled with doped polysilicon or implanted and annealed to create a "backside" electrode
- UC Santa Cruz/Naval Research Lab is exploring an alternate process involving cleaving and atomic layer deposition

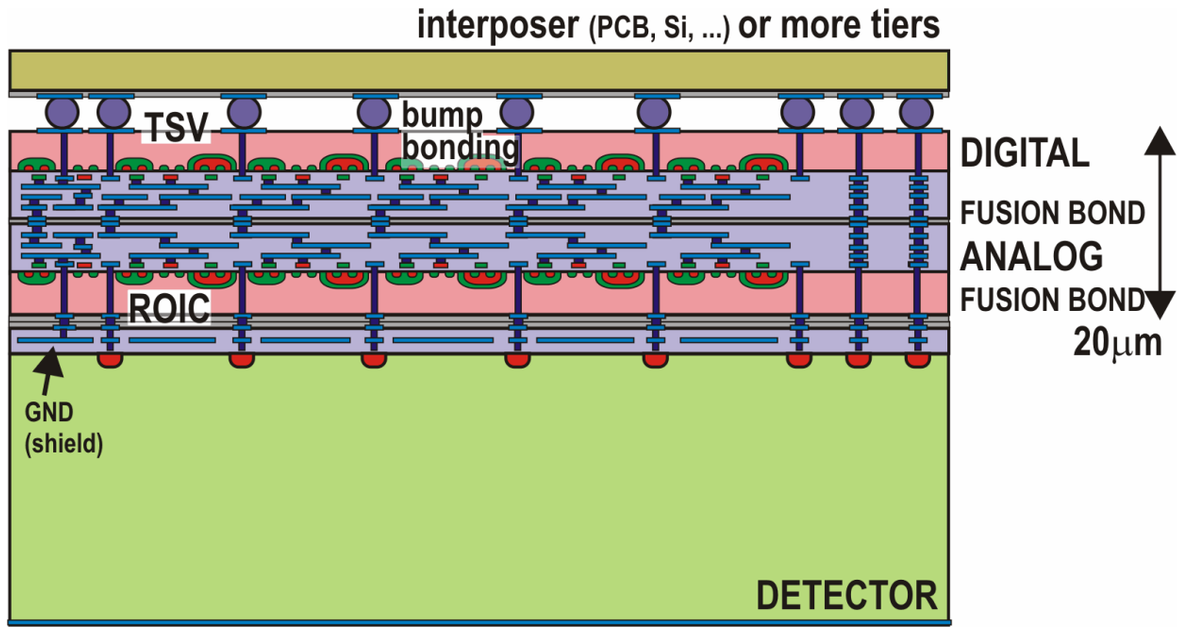


VTT Active Edge Sensor



after cleaving

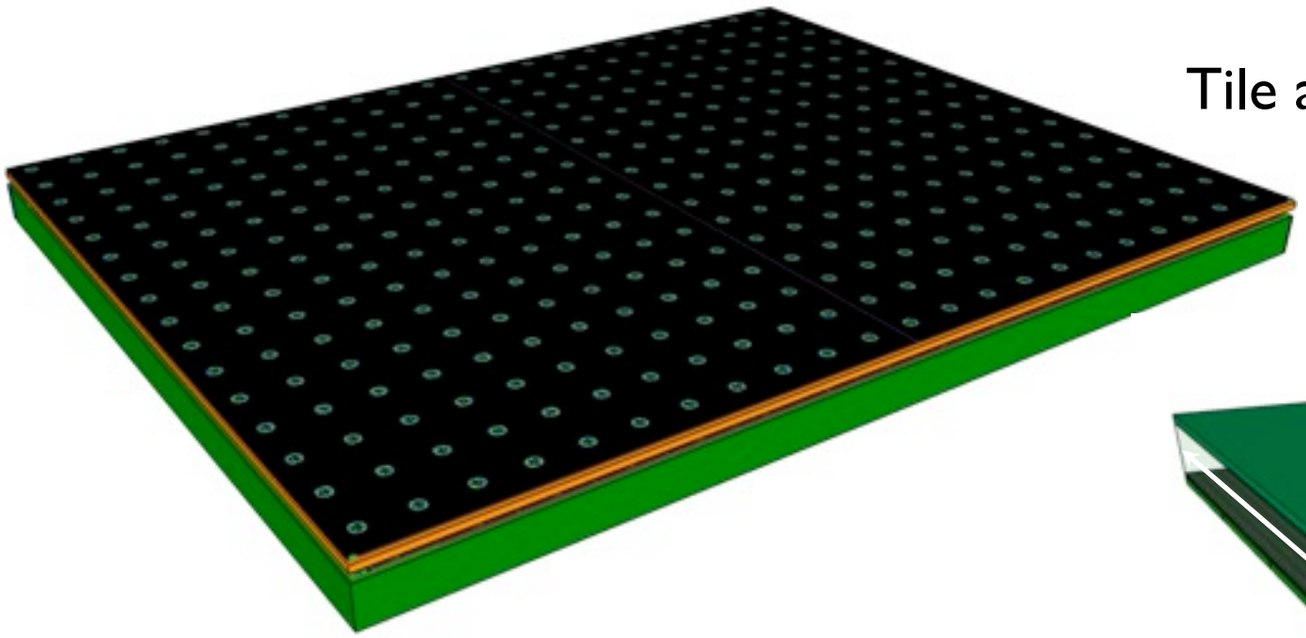
The goal of this work is to combine active edge technology with 3D electronics and oxide bonding with through-silicon vias to produce fully active tiles.



- Driven by CMS track trigger needs (100's of m2 of 3D pixelated sensors)
- These tiles can be used to build large area pixelated arrays with good yield and low cost because the only bump bonds are large pitch backside interconnects.
- Fine pitch bonds to the sensor are made using wafer to wafer oxide bonding

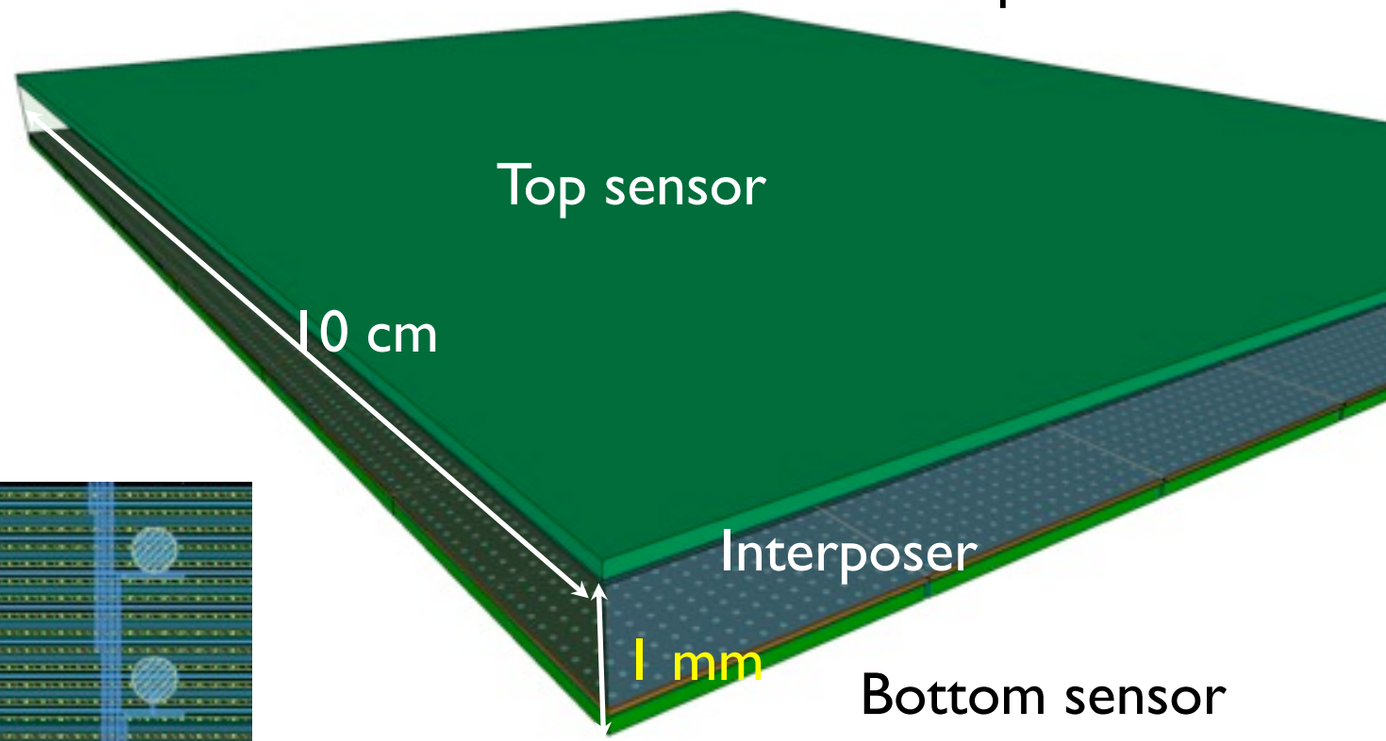
  Collaborators: G. Deptuch, J. Thom, E. Sawyer, S. Parker, C. Kenny, R. Lipton, A. Shenai, M. Trimpl, M. Johnson, Z. Ye, F. Kahlid, S. Cihangir

Tiled Active Edge Modules

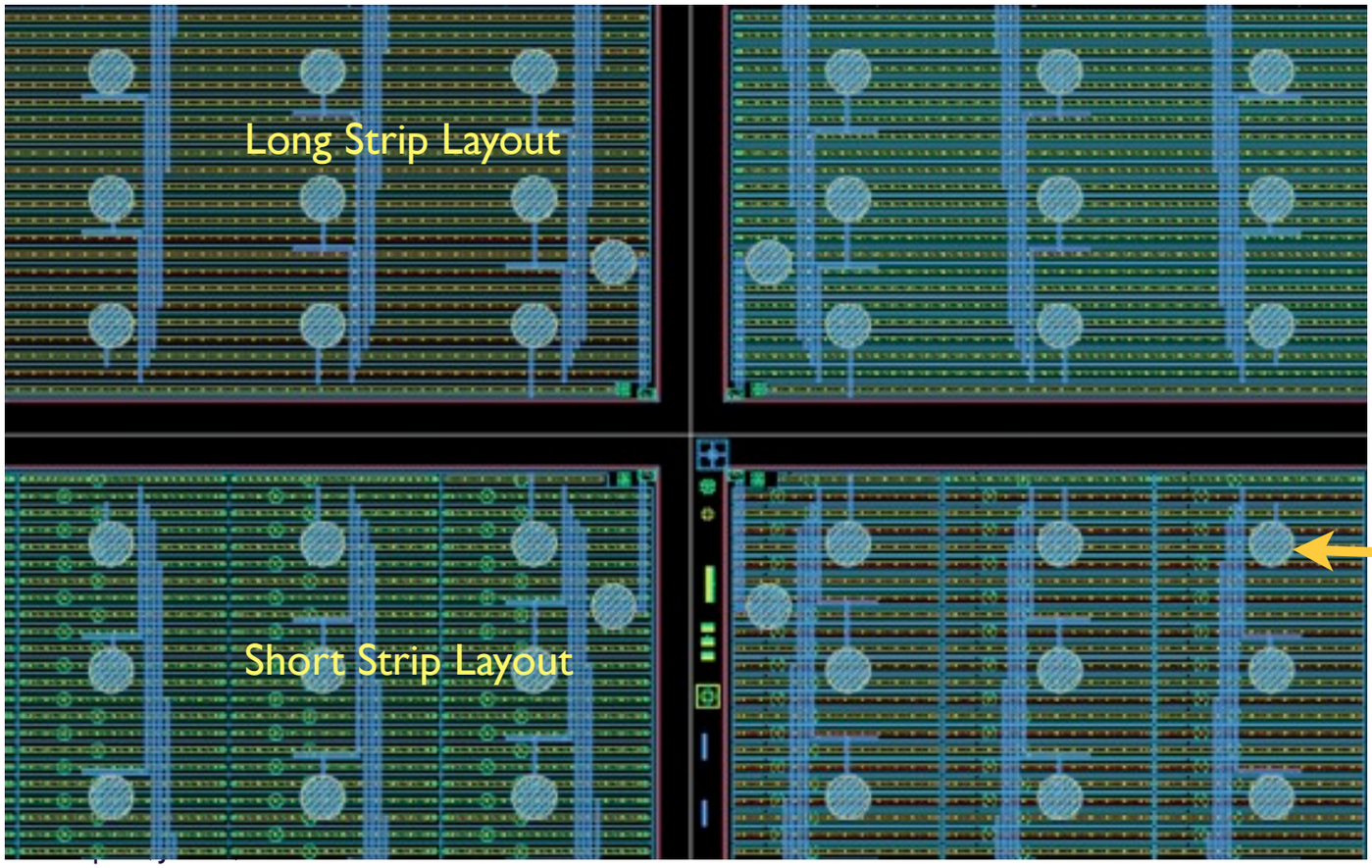


Tile after handle wafer removal and singulation

Full Module with interposer and top sensor



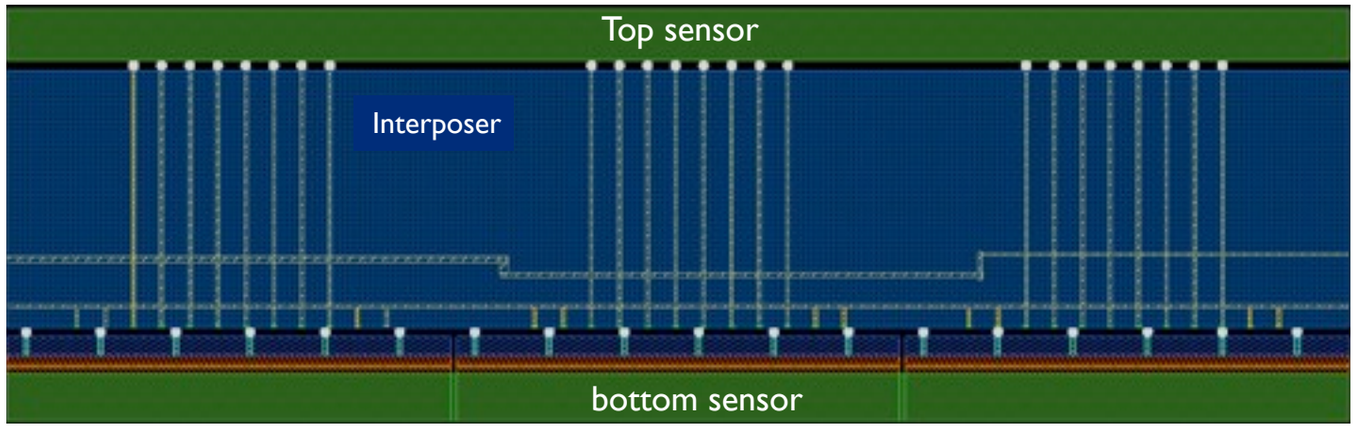
- Design of sensors is complete
- Design of dummy ROIC is complete



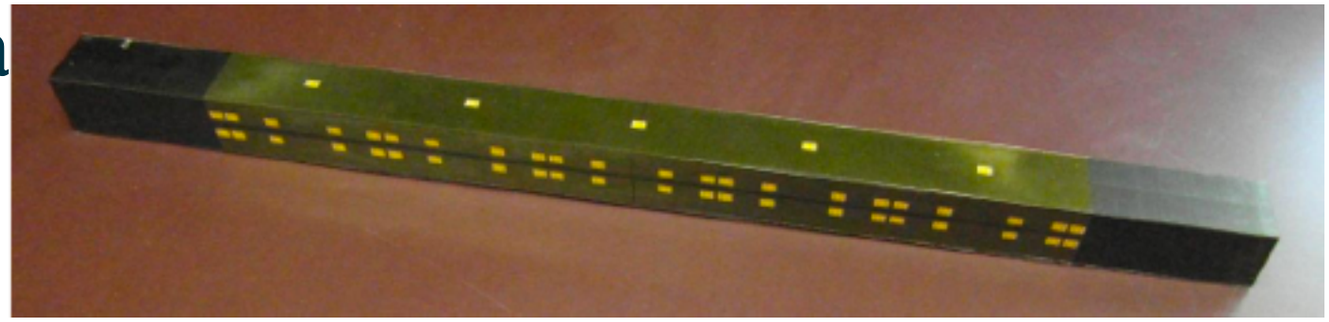
Bonding, Module and Rod Mechanics

- The track trigger detector requires low mass modules which
  - Transmit analog from top to bottom sensor
  - Connect chips and send data off-detector
- We are developing mechanical prototypes of:
  - Interposers based on pcb technology matched to silicon cte
  - Carbon fiber support beams for rods
  - Bump bonded modules arrays
  -

Top bump bonds



bottom bump bonds



Opportunities for Collaboration

- Testing of the VICTR chip
  - Stack assembly and beam tests
- Stack assembly
  - Bump bonding
  - Interposer
- VICTR2
  - Design and Simulation
  - Testing
- Active edge devices
  - Design of test infrastructure
  - Device testing
  - Beam tests
- Off-detector track formation
- Design and simulation
- Mechanics
  - Rod design